DUSTY

User's Guide

ITM-DYPA-B-02: Dusty PCB Ant.
ITM-DYUF-B-02: Dusty U.FL Conn.

Outline

Illustrations

Tables

Revisions

REVISION	DATE	DESCRIPTION	STATUS	AUTHOR	REVISER
Ver. 1.0	31/01/2017	First release	Final	info@midatronics.com	
Ver. 1.1	04/07/2017	FCC	Final	info@midatronics.com	SB
Ver. 1.4	13/07/2017	Certificazioni	Final	info@midatronics.com	
Ver. 1.5	27/07/2017	Radiation plot	Final	info@midatronics.com	
Ver. 1.6	09/11/2017	Part num. update	Final	info@midatronics.com	
Ver. 1.7	08/01/2019	Update Logo	Final	info@midatronics.com	ME
Ver. 1.8	21/03/2019	Updated Company Info	Final	info@midatronics.com	AC

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1. Introduction

1.1. Description

This document describes the Dusty module. Dusty is a SmartMesh IP™PCBA product incorporating the LTC5800-IPM SoC running Dust's embedded SmartMesh IP™™ networking software. The Dusty module comes complete with an onboard PCB antenna or U.FL antenna connector, crystals and modular RF certifications.

The Dusty module is produced in two flavors:

- **Dusty PCB-Ant (On board PCB Antenna)**
- **Dusty U.LF Ant Conn (On board U.LF antenna connector)**

Main features

- PCBA module with PCB antenna or U.FL connector
- Integrated 2.4 GHz, IEEE 802.15.4e System-on-Chip, complete with Embedded SmartMesh Networking Software
- >99.999% Network Reliability in the Most Challenging RF Environments ‣ Sub 50µA Routing Nodes
- Serves as either a Wireless Mote, Embedded Manager, or Access Point Mote in a SmartMesh IP™ network depending on the loaded firmware

2. System overview

2.1. SmartMeshIP™ Technology overview

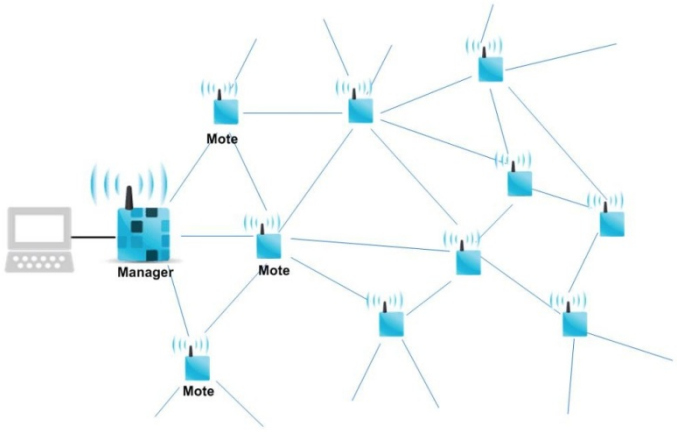

Figure 1 Mesh network

A SmartMesh IP™ network consists of a highly scalable self-forming multi-hop mesh of wireless nodes, known as motes, and an Access Point mote that connects the motes to the Network Manager, monitoring and managing network performance and security, and acting as a bridge between the host application and the wireless network. Motes are capable of two way communication and they collect and relay data.

2.2. Dusty in a SmartMesh IP™ network

With SmartMesh IP™ time-synchronized networks, all motes in the network may route, source or terminate data, while providing many years of battery powered operation. SmartMesh IP™ is a highly flexible network with proven reliability and low power performance in an easy-to-integrate platform.

The Dusty's behavior in a SmartMesh IP™ network is determined by the choice of SmartMesh IP™ network software loaded: Wireless Mote, Embedded Manager, or Access Point Mote.

The SmartMesh IP™ software provided with the Dusty is fully tested and validated, and is readily configured via a software Application Programming Interface.

For more information on SmartMeshIP™ visit the following site:

https://www.analog.com/en/products/rf-microwave/wireless-sensor-networks/smartmesh-ip.html

2.3. SmartMeshIP™ Features

Ultra low-power network

The network can run on batteries, energy harvesting, or line power

High network reliability

>99.999% network reliability even in harsh RF environments

IPv6 addressability

Combines 6LoWPAN with IEEE 802.15.4e

Comprehensive security management

Allows you to configure NIST-certified AES-128 based security to meet your requirements

Flexible configuration

Network parameters can be selected to match specific system requirements (power / latency / bandwidth)

Fully tested network stack and manager software

Application programming interfaces are used to communicate with and to configure the product - no user networking code necessary.

2.4. LTC5800-IPM - SmartMesh IP™ Wireless 802.15.4e System-on-Chip

The Dusty module is based on Analog Devices LTC5800-IPM SmartMesh IP™ Wireless 802.15.4e System-on-Chip.

The LTC5800-IPM provides a highly integrated, low power radio design as well as an ARM Cortex-M3 32-bit microprocessor running SmartMesh IP™ embedded networking software.

For more information on LTC5800-IPMvisit the following site:https://www.analog.com/en/products/ltc5800-ipm.html

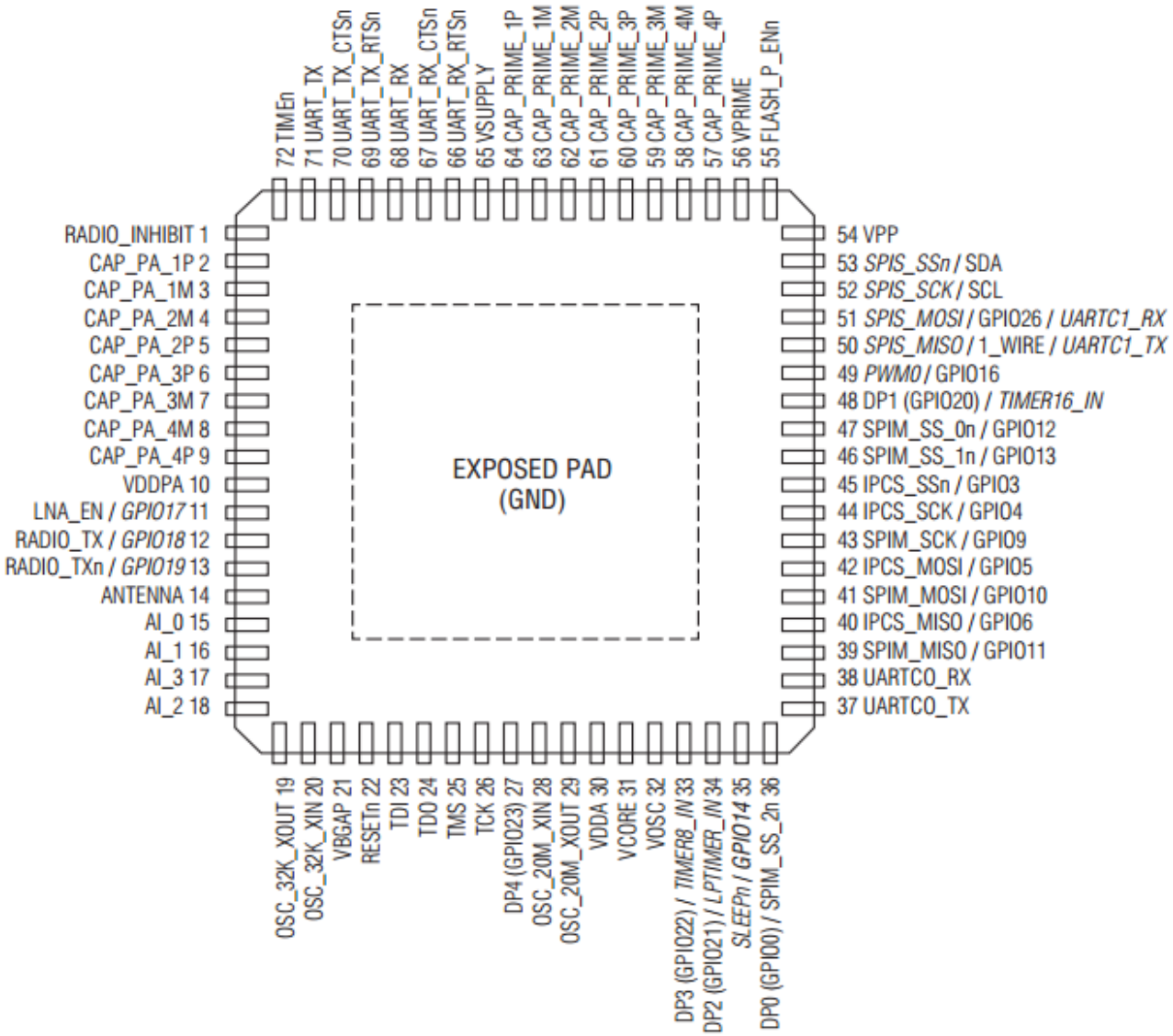

Figure 2 LTC 5800 IPM

2.5. Block Diagram

An overview of the functions of the DUSTYmodule is shown in the figure below:

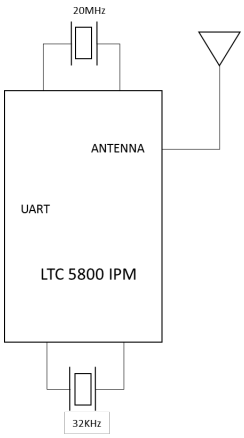

Figure 3 Dusty Block diagram

2.6. Module Specifications

For a more detailed specification refer to the original LTC5800 datasheet:

https://www.analog.com/media/en/technical-documentation/data-sheets/5800ipmfa.pdf

3. Connectors

The following picture shows the Dusty module pinout. The module is seen from the top (top view) but the two Power Supply pads are on the bottom side of the module. The pins and the pads position is the same for both module types.

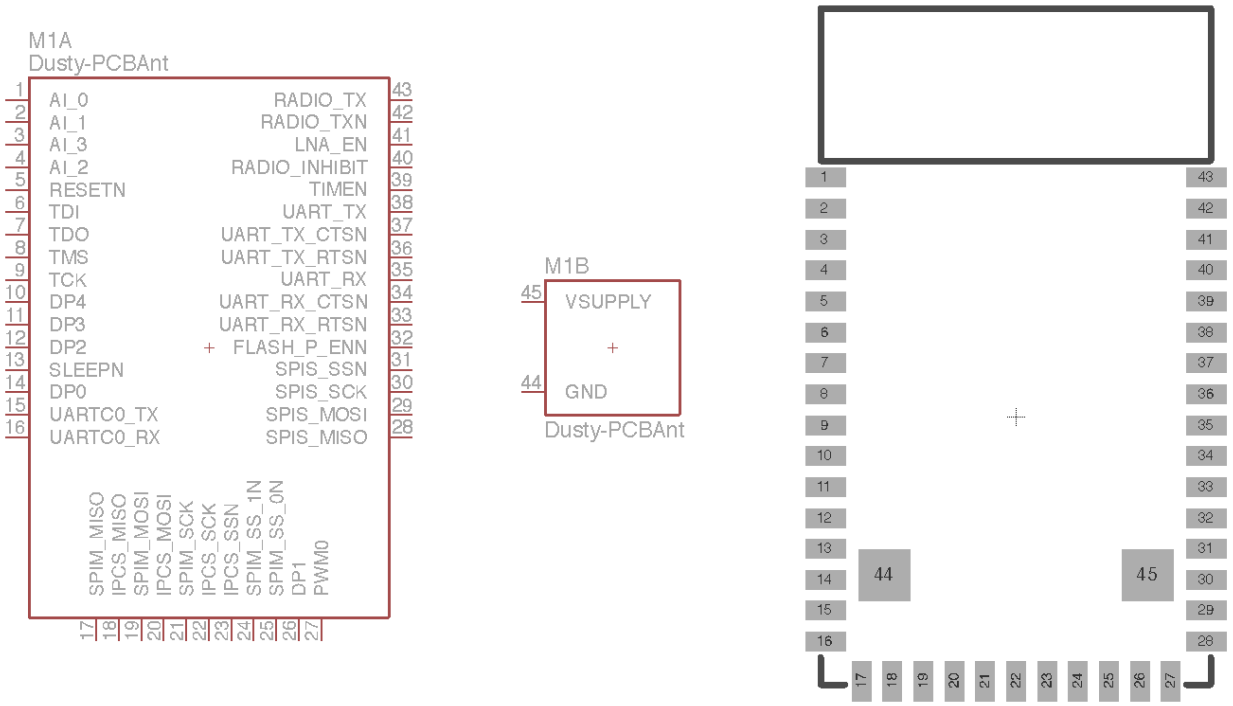

Figure 4 Dusty pinout TOP View

The signals of the pins depend on the firmware loaded on the module.

Dusty Pin	SoC Pin	I/O	Pull	Description
		LTC5800-IPR	LTC5800-IPM	LTC5800-IPA
		Embedded Manager	Moto on chip	Access Point Mote
1	15	AI_0	AI_0	RESERVED
2	16	AI_1	AI_1	RESERVED
3	17	AI_3	AI_3	RESERVED
4	18	AI_2	AI_2	RESERVED
5	22	RESETn	RESETn	RESETn
6	23	TDI	TDI	TDI
7	24	TDO	TDO	TDO
8	25	TMS	TMS	TMS
9	26	TCK	TCK	TCK
10	27	DP4	DP4 / GPIO23 / TIMER8_EXT	DP4
11	33	DP3	DP3 / GPIO22 / TIMER8_EXT	RESERVED
12	34	DP2	DP2/ GPIO21 / LPTIMER_EXT	RESERVED
13	35	SLEEPN	SLEEPn / GPIO14	RESERVED
14	36	DP0	DP0 / GPIO0 / SPIM_SS_2n	RESERVED
15	37	UARTC0_TX / EB_IO_LE0	UARTC0_TX	UARTC0_TX
16	38	UARTC0_RX / EB_DATA_1	UARTC0_RX	UARTC0_TX
17	39	SPIM_MISO	SPIM_MISO / GPIO11	SPIM_MISO
18	40	IPCS_MISO	IPCS_MISO / TIMER16_OUT / GPIO6	IPCS_MISO
19	41	SPIM_MOSI	SPIM_MOSI / GPIO10	SPIM_MOSI
20	42	IPCS_MOSI	IPCS_MOSI / TIMER16_EXT / GPIO5	IPCS_MOSI
21	43	SPIM_SCK	SPIM_SCK / GPIO9	SPIM_SCK
22	44	IPCS_SCK	IPCS_SCK / TIMER8_EXT / GPIO4	IPCS_SCK
23	45	IPCS_SSn	IPCS_Ssn / LPTIMER_EXT / GPIO3	IPCS_SSn
24	46	SPIM_SS_1n	SPIM_SS_1n / GPIO13	SPIM_SS_1n
25	47	SPIM_SS_0n	SPIM_SS_0n / GPIO12	SPIM_SS_0n
26	48	DP1	DP1 / GPIO20 / TIMER16_EXT	RESERVED
27	49	PWM0	PWM0 / TIMER16_OUT / GPIO16	PWM0
28	50	UARTC1_TX	SPIS_MISO / UARTC1_TX / 1_WIRE	RESERVED
29	51	UARTC1_RX	SPIS_MOSI / UARTC1_RX / GPIO26	RESERVED
30	52	EB_IO_WEn	SPIS_SCK / SCL	RESERVED
31	53	EB_IO_OEn	SPIS_Ssn / SDA	RESERVED
32	55	FLASH_P_Enn / EB_IO_LE1	FLASH_P_ENn	FLASH_P_ENn
33	66	UART_RX_RTSn	UART_RX_RTSn	RESERVED
34	67	UART_RX_CTSn	UART_RX_CTSn	RESERVED
35	68	UART_RX	UART_RX	UART_RX
36	69	UART_TX_RTSn	UART_TX_RTSn	RESERVED
37	70	UART_TX_CTSn	UART_TX_CTSn	RESERVED
38	71	UART_TX	UART_TX	UART_TX
39	72	TIMEn	TIMEn	TIMEn
40	1	RADIO_INHIBIT	RADIO_INHIBIT	RESERVED
41	11	LNA_EN	LNA_EN / GPIO17	LNA_EN
42	13	RADIO_TXn	RADIO_Txn / GPIO19	RADIO_TXn
43	12	RADIO_TX	RADIO_TX / GPIO18	RADIO_TX
44	EP	GND	GND	GND
45	65	VSUPPLY	VSUPPLY	VSUPPLY

Table1 Pinout Description

Name	I/O	Pull	Description
AI_n	I	-	Analog Input n
DPn	I/O	-	General Purpose Digital I/O n
TDI	I	UP	JTAG Test Data In
TDO	I	-	JTAG Test Data Out
TMS	I	UP	JTAG Test Mode Select
TCK	I	DOWN	JTAG Test Clock
UARTCn_TX	O	-	CLI UART n Transmit
UARTCn_RX	I	UP	CLI UART n Receive
SPIM_MISO	I	-	SPI Master (MISO) Master In Slave Out Port
SPIM_MOSI	O	-	SPI Master (MOSI) Master Out Slave In Port
SPIM_SCK	O	-	SPI Master (SCK) Serial Clock Port
SPIM_SS_1n	O	-	SPI Master Slave Select 1, Active Low
SPIM_SS_0n	O	-	SPI Master Slave Select 0, Active Low
RESETn	I	UP	Reset Input, Active Low
SLEEPN	I	-	Deep Sleep, Active Low
IPCS_MISO	O	-	SPI Flash Emulation (MISO) Master In Slave Out Port
IPCS_MOSI	I	-	SPI Flash Emulation (MOSI) Master Out Slave In Port
IPCS_SCK	I	-	SPI Flash Emulation (SCK) Serial Clock Port
IPCS_SSN	I	-	SPI Flash Emulation Slave Select, Active Low
SPIS_MISO	O	-	SPI Slave (MISO) Master In Slave Out Port
SPIS_MOSI	I	-	SPI Slave (MOSI) Master Out Slave In Port
SPIS_SCK	I	-	SPI Slave (SCK) Serial Clock Port
SPIS_SSN	I	-	SPI Slave Select, Active Low
UART_RX	I	-	UART Receive
UART_TX	O	-	UART Transmit
UART_TX_RTSn	O	-	UART Transmit (RTS) Request to Send, Active Low
UART_TX_CTSn	I	-	UART Transmit (CTS) Clear to Send, Active Low
UART_RX_RTSn	I	-	UART Receive (RTS) Request to Send, Active Low
UART_RX_CTSn	O	-	UART Receive (CTS) Clear to Send, Active Low
FLASH_P_ENn	I	UP	Flash Program Enable, Active Low
EB_DATA_n	I/O	-	External Bus Data Bit n
EB_IO_LE0	O	-	External Bus I/O Latch Enable 0 for External Address Bits A[25:18]
EB_IO_LE1	O	-	External Bus I/O Latch Enable 1 for External Address Bits A[17:10]
EB_IO_LE2	O	-	External Bus I/O Latch Enable 2 for External Address Bits A[9:2]
EB_ADDR_x	O	-	External Bus Address Bit x (0 or 1)
EB_IO_CS0n	I	-	External Bus Chip Select 0
EB_IO_WEn	O	-	External Bus Write Enable Strobe
EB_IO_OEn	O	-	External Bus Output Enable Strobe
GPIO_n	I/O	-	General Purpose Input Output n
PWM0	O	-	Pulse Width Modulator 0
TIMER8_EXT	I	-	External Input to 8-Bit Timer/Counter
TIMER8_OUT	O	-	8-Bit Timer/Counter Match Output
TIMER16_EXT	I	-	External Input to 16-Bit Timer/Counter
TIMER16_OUT	O	-	16-Bit Timer/Counter Match Output/PWM Output
1_WIRE	I/O	-	1 Wire Master
LPTIMER_EXT	I	-	External Input to Low Power Timer/Counter
TIMEn	I	-	Time Capture Request, Active Low
RADIO_INHIBIT	I	-	Radio Inhibit
LNA_EN	O	-	External LNA Enable
RADIO_TXN	O	-	Radio TX Active (External PA Enable/Switch Control), Active Low
RADIO_TX	O	-	Radio TX Active (External PA Enable/Switch Control)

Table2 Signal short Description

4. Usage

This chapter describes how to connect, configure and interact with the Dustymodule.

4.1. Power supply

Dusty is powered from a single pin, VSUPPLY, whichpowers the I/O cells and is also used to generate internalsupplies. Eterna®'s two on-chip DC/DC converters minimizeenergy consumption while the device is awake. Toconserve power the DC/DC converters are disabled whenthe device is in low-power state. Integrated power supplyconditioning, including the two integrated DC/DC convertersand three integrated low-dropout regulators, providesexcellent rejection of supply noise. Eterna®'s operatingsupply voltage range is high enough to support directconnection to lithium-thionyl chloride (Li-SOCl2) sourcesand wide enough to support battery operation over a broadtemperature range.

5. Board layout

The following picture shows the dimensions of the two Dusty types: Dusty PCB-Ant (integrated PCB Antenna) and Dusty U.FL Ant Conn (integrated U.FL antenna connector)

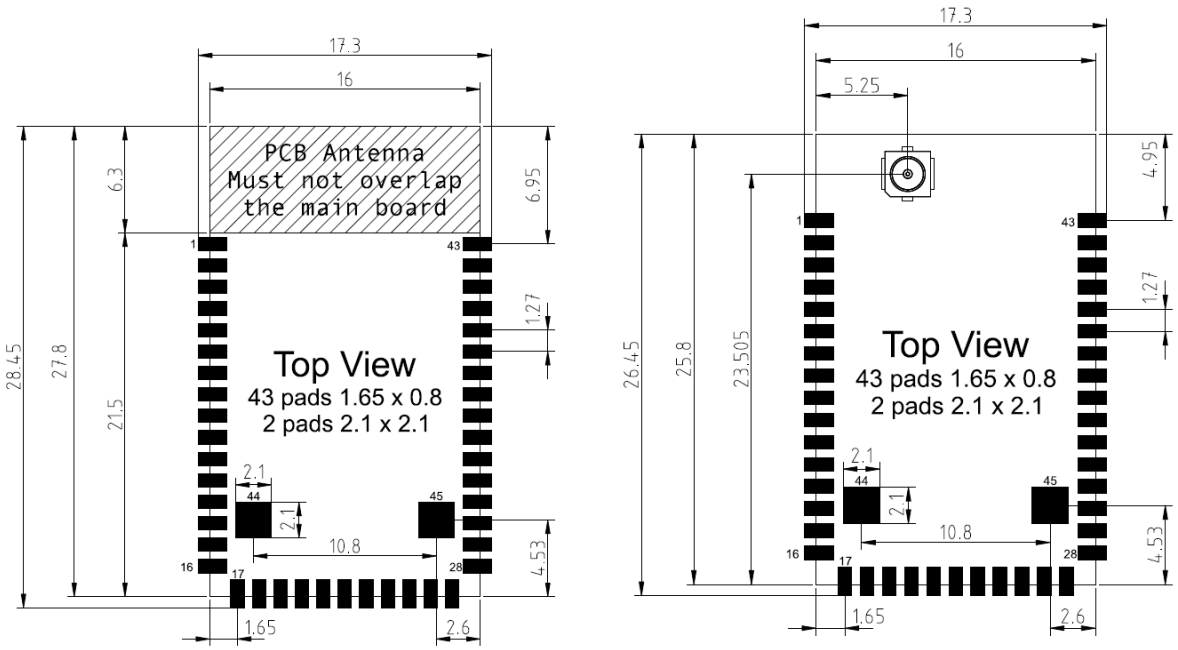

Figure 5 Dusty dimensions

5.1. Dusty PCB-Ant mounting suggestion

The Dusty PCB-Ant provides an integrated PCB Antenna, therefore it is really important that the module is mounted on the hosting board in the proper way. No other components should be mounted around the antenna.

The following picture provides an example of how the module should be mounted on a hosting board.

Note how the antenna juts out of the hosting board.

Figure 6 Dusty mounting sample

6. Radiation pattern plots of the Dusty PCB-Ant module

The following figures show the radiation pattern of the Dusty PCB-Ant module mounted on the Dragofly of Figure 6.

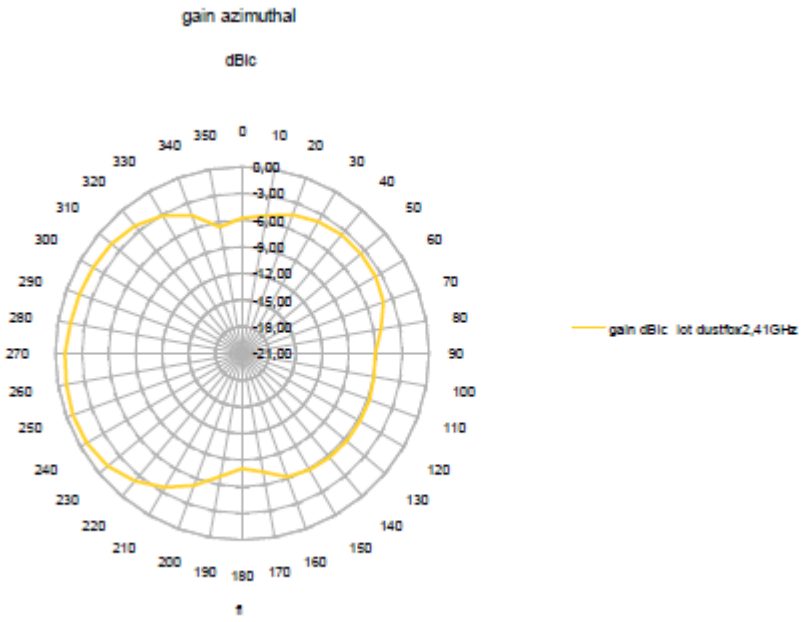

Figure 7Dusty PCB Ant. Radiation pattern : gain azimuthal

Max	-0,7	dBic
Min	-0,8	dBic
Avg	-3,8	dBic
Mdn	-4,2	dBic
Eff	-0,1	dB

Table 3 Radiation gain azimuthal

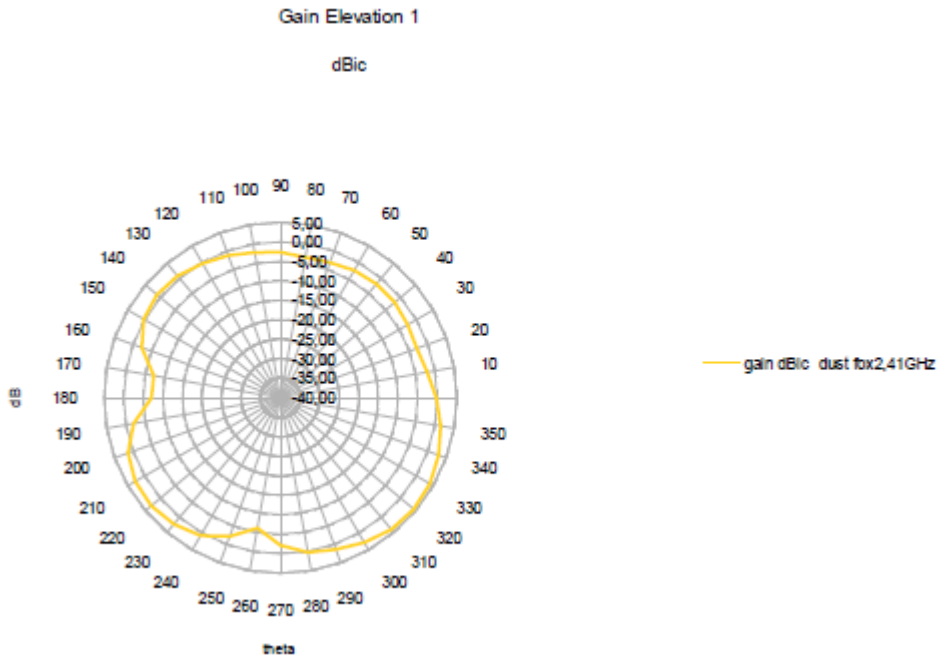

Figure 8Dusty PCB Ant. Radiation pattern : gain elevation

Max	-4,4	dBic
Min	-7,2	dBic
Avg	-0,1	dBic
Mdn	-0,7	dBic

Table 4 Radiation gai elevation

7. Firmware Upload

Dusty's behavior in a SmartMesh IP™ network is determined by the choice of SmartMesh IP™ network Firmware loaded:

- Wireless Mote
- Emanager
- Access Point Mote

By default Dusty will have the Wireless Mote firmware preloaded with some predefined characteristics.

If the user wants to change the firmware or change some parameters it is necessary to upload the firmware. The firmware can be downloaded from: https://my.analog.com/

In order to download the firmware, the customer must sign in and ask the local sales team the firmware. They'll post the file to be downloaded from the MyAnalog website and uploaded to Dusty.

The firmware upload requires the following tools:

- Firmware to be uploaded
- Eterna®DC9010 Serial Programmer
- Dusty connector used to connect the module to the Eterna® Serial Programmer
- PC running Windows and USB 2.0 or USB 3.02 port
- ESP software (downloadable from https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/dc9010b.html)

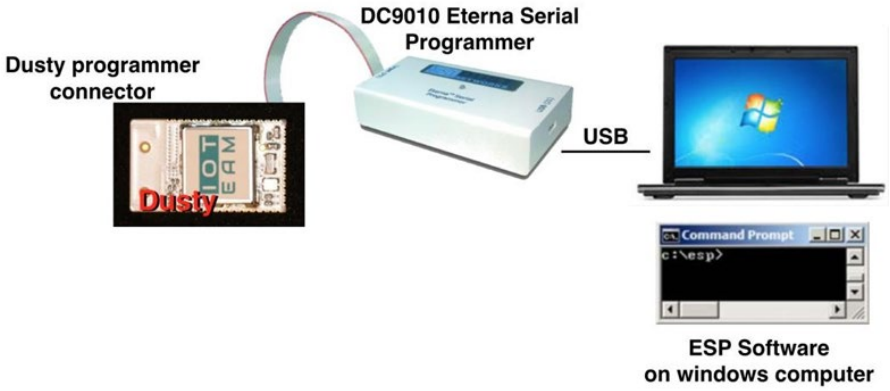

Figure 9 Required tools to upload firmware

For the detailed procedure and more detailed information see the following document:https://www.analog.com/media/en/technical-documentation/user-guides/Eterna_Serial_Programmer_Guide.pdf

8. Software Development

TheARMCortex-M332-bitmicroprocessor,insidetheLTC®5800-IPMSoC,normallyruns the provided SmartMesh IP™ network software, but it can be customized and allows the user to develop their own software and add functionality to themodule.

The On-Chip Software Development Kit (OCSDK) allows you to write applications directly on the LTC5800-IP SoC on top of the SmartMesh IP™ network protocol stack.

The SmartMesh IP™ stack and the device drivers are provided as pre-compiled libraries. Your mote application links against them, and can then be loaded into the Dusty board.

In order to develop a custom firmware to be uploaded to the Dusty module, the following tools are necessary:

- A Windows PC
- IAR Embedded Workbench for ARM. Note that the kickstart addition will not work with the OCSDK

- On-Chip Software Development Kit (OCSDK) downloadable from Github (https://github.com/dustcloud/onchipsdk)
- Library files from Analog to be copied into the OCSDK
- Python installed on the PC
- Programming and debugging tools (optional)

All the details and instructions about the development of custom firmware for the LTC5800-IPM SoC embedded in the Dusty module may be found at the following link: https://dustcloud.atlassian.net/wiki/display/OCSDK/

9. References and Useful Links

9.1. Data sheets and documents

- https://www.analog.com/en/products/rf-microwave/wireless-sensor-

networks/smartmesh-ip.html

- https://www.analog.com/en/products/ltc5800-ipm.html
- https://www.analog.com/media/en/technical-documentation/data-sheets/5800ipmfa.pdf

9.2. Tools

- https://www.analog.com/media/en/technical-documentation/user-guides/eterna_serial_programmer_guide.pdf
- https://dustcloud.atlassian.net/wiki/display/OCSDK/
- https://www.iar.com/iar-embedded-workbench/arm/

9.3. WebSites

- MIDATRONICS S.r.l. - www.midatronics.com
- Analog Devices - www.analog.com

FCC Statement:

This equipment has been tested and found to comply with the limits for Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
Reorient or relocate the receiving antenna.
Increase the separation between the equipment and receiver.
Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Note: Modifications to this product will void the user's authority to operate this equipment.

9.4. RF RadiationExposure Statement:

1. This Transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
2. This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body.

9.5. FCC Information to OEM integrator

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user manual of the end product.
The user manual which is provided by OEM integrators for end users must include the following information in a prominent location.

1. To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter, except in accordance with FCC multi-transmitter product procedures.
2. Only those antennas with same type and lesser gain filed under this FCC ID number can be used with this device.
3. The regulatory label on the final system must include the statement: "Contains FCC ID: 2AL5T - DUSTY" or using electronic labeling method as documented in KDB 784748.
4. The final system integrator must ensure there is no instruction provided in the user manual or customer documentation indicating how to install or remove the transmitter module except such device has implemented two-ways authentication between module and the host system.

10. Certifications

ETSIEN 301 489-1 V2.1.1 (Europe)

ETSI EN 301 489-17V3.1.1 (Europe)

EN 61000-3-2:2014 (Europe)

EN 61000-3-3:2013 (Europe)

ETSI EN 300328V2.1.1 (Europe)

FCC CFR47 Part 15 (/US)

RoHS 2011/65/EU